CURRICULUM VITAE

Itamar Levi

Jan, 2020

Name: Itamar Levi

Phone: +972 / 0503-460-385

Email: itamar.levi@biu.ac.il

Address (work): Faculty of Engineering, building 1102 - room 410A , Bar- Ilan University, Ramat- Gan, 52900, Israel.

Address (home): Ya'ara 16, Lehavim 8533800, Israel.

Brief profile

My research activities combine logical-, electrical- and physical- foundations of secure-hardware. Spanning from theoratical analysis and evaluation, to design, architectures and algorithms of cryptographic primitives. I work with hardware, embedded software-hardware systems and combinations of the above. My overarching goal is to respond to today's and tomorrow's physical security challanges which, in many cases, require that we tackle existing hardware security mechanisms to identify security flaws. The target environments we face are constraining, low on resources and highly exposed to adversaries (e.g. IoT, Automotive). As such my agenda is not only to be able to provide verifiable *physical*-security but also to do so in a resource efficient way (perf., energy, area and reliability).

Present position

Senior Lecturer, 2019 – present, Bar-Ilan University (BIU), Faculty of Engineering, Computer Engineering. A member of EnICS-LABs (Emerging Nano-scaled Integrated-Circuits and Systems).

Education and Prior-Positions

Post-Doctoral Researcher, 2017 – 2019, Université catholique de Louvain (UCL), ICTEAM Institute – UCL Crypto Group & Electronics Circuits and Systems group (ECS).

Promotor: Prof. Francois-Xavier Standaert. Co-Promotor: Prof. David Bol

Main Research Activity: Working on the European-Research-Council (ERC) Horizon-2020 grant project, SWORD (Security Without Obscurity for Reliable Devices). Research topics: cross-layer security and optimization, from technology and hardware (ASICs, FPGAs ..) to architecture, algorithms and software implementation. I have been working on the interactions between cryptographic constructions (e.g. authenticated

encryption, randomness generators) and the physical world (hardware security and implementation).

Ph.D, 2014 – 2017, Faculty of Engineering, Bar-Ilan University (BIU), Ramat-Gan, Israel.

Advisor: Prof. Alexander Fish and Dr. Osnat Keren.

Subject: Hardware Security, Side-Chanel Leakage Protection, Dedicated Secured Cryptographic Circuits and Digital Circuits Design techniques.

M.Sc, 2011 – 2013, Department of Electrical and Computer Engineering, Faculty of Engineering, Ben-Gurion University (BGU), Beer-Sheva, Israel. *Cum Laude.*

Advisor: Prof. Alexander Fish and Eugene Paperno.

Subject: Energy Efficient and High Performance Dual Mode Logic (DML) family.

B.Sc, 2008 – 2011, Department of Electrical and Computer Engineering Faculty of Engineering, Ben-Gurion University (BGU), Beer-Sheva, Israel. *Cum Laude.*

Achievements and Awards

- 2015 - Rector's prize for outstanding academic achievements and excellent Ph.D research.
- 2012 - Direct Masters-In-Science *fast-track* program for excellent students with an academic horizon (B.Sc. and M.Sc. in 5 instead of 6 years of study).
- 2012 - *cum laude* award for B.Sc.
- 2012 - *cum laude* award for the 1st year of the M.Sc degree.

Conferences Committee:

IEEE HOST (Hardware Oriented Security and Trust)
– Technical Program Comitee (TPC)
ASHES (Attacks and Solutions in Hardware Security)
– Program Comitee (PC)
MAL-IoT19 - Malicious Software and Hardware in the Internet of Things
–Technical Program Comitee (TPC)

Reviewer for Journals and Conferences:

Journals IEEE Transactions on Circuits and Systems II Journal;
IEEE Transactions on Circuits and Systems I Journal;
Elsevier Micro-Electronics Journal;
IEEE Transactions on VLSI.
Elsevier Integration, The VLSI Journal

	IEEE sensors Journal
	JLPEA, Journal of Low-Power, Electronics and Applications
	IEEE Access Journal
Conferences	IEEE International Symposium on Circuits and Systems (ISCAS);
	IEEE International Conference on Electronics, Circuits and Systems (ICECS);
	IEEE Sensors Conference; IEEE International Midwest
	HOST 2018 – Technical Program Comitee (TPC)
	ASHES 2018 – Program Comitee (PC)

Patents and Applications

[1] **I. Levi**, R. Giterman, M. Visentowsky, Y. Waitzman, O. Keren and, A. Fish, "SECURED MEMORY", Provisional Application, 2017. Number 67247, Ehrlich Ref. 76032, BIRAD Ref. 7506.

[2] **I. Levi**, O. Keren, and A. Fish, "Methodology For Secured Hardware by Insertion of Data-Dependent Delays", Provisional application, May 2016.

[3] **I. Levi**, O. Keren, and A. Fish. *Pseudo-asynchronous digital circuit design*. U.S. Patent Application 16/312,317, 2019.

[4] **I. Levi**, O. Keren, and A. Fish. *Data-dependent delay circuits*. U.S. Patent Application 15/636,902, 2018.

[5] M. Avital, **I. Levi**, O. Keren and A. Fish, "Randomized Logic against side channel attacks", Patent Application, September 2015.

[6] M. Avital, **I. Levi**, O. Keren, and A. Fish "Multi-Topology Logic Gates", PCT application No: PCT/IL2015/050446, August 2015.

[7] A. Fish, A. Kaizerman, S. Fisher, and **I. Levi**, "Device and method for dual-mode logic," patent No: 8,901,965, Granted December 2014

[8] A. Fish, A. Kaizerman, **I. Levi**, and S. Fisher, "Design of dual mode logic circuits," application No: PCT/IL2013/050111, August 2013.